Testing Serial Data Signals

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Introduction

Within the last few years a variety of high speed serial data protocols have been proposed to replace older, lower speed parallel busses. New standards include RapidIO, Serial ATA, XAUI, PCI-Express, high speed fibrechannel and more. Many of these borrow test methods and specifications from older serial data standards used by long haul carriers for telecom applications--standards such as OC-12 and OC-48. But now the data transmission may be from chip to chip, or between a one device and another nearby device rather than between two cities. These shorter data paths make it easier to send high bit rates, but such high rates also make it mandatory that the engineer closely test a design to make sure it meets the tight specifications of the standard.This article will discuss new methods for more accurate acquisition of serial data streams, improvements in visually inspecting them through advances in eye patterns and several techniques for improved accuracy in numeric measurements. The good news is that every serial data standard has the same basic types of tests-- for basic signal parameters (signal amplitude, rise time, bit length, etc), jitter/timing measurements (clock to data jitter, pulse width jitter, frequency stability and so forth) and mask tests (making sure the data bits fit inside a specified shape). So though each standard has specific differences from the others, the general test methods are very similar.

Advances in Signal Acquisition

The first step in testing a serial data signal is to acquire an accurate representation of what the signal looks like. In many cases, the initial contact of the test system with the signal is through a probe. Until recently, the highest bandwidth differential probe was 3.5 GHz—a marginal method for acquiring signals in the range of 2.5 to 3.5 gigabits per second. In recent months several new high bandwidth differential probes have been introduced including the 7.5 GHz and 4.0 GHz WaveLink models from LeCroy. These probes have a combination of low capacitance and inductance along with high bandwidth to provide industry leading ability to capture high speed differential signals with maximum signal integrity. A substantial advantage of these probes is a divide by two attenuation compared to factors of divide by 10 and 6.25 in other probes. This means more of the signal amplitude is preserved.

The probe passes the signal into the oscilloscope. Recent technology advances have brought the state of the art in real time scope performance to 6 GHz analog bandwidth for the front end amplifier, 20 GS/s sampling rate for the ADC (20 samples per nanosecond) and 100 million points of acquisition memory. This combination allows the oscilloscope to capture a continuous signal for up to 5 milliseconds at 20 GS/s. The ability to capture such a long continuous series of bits from a serial data signal and analyze them using a the X-Stream processing engine with calculating power of one GFLOP (one billion floating point calculations per second) enables new, more accurate methods of measuring key characteristics of serial data signals.

Eye Diagrams

Often, the first type of analysis an engineer uses in determining how well a serial data circuit is working is to look at an eye diagram. Many years ago, the eye diagram test started as a quick-and-dirty method to visually check the quality of transmission in a serial data stream. In its earliest use, an oscilloscope was triggered on

the clock which was driving the system and the user simply viewed the 1's and 0's on the scope screen, visually examining the amount of timing jitter and amplitude variation. In its next iteration, standard test masks were defined. A signal which intruded into the mask violated the standard. Typical masks have an "eye" in the center in addition to regions at the top and bottom which test for overshoot/undershoot. In the past, the oscilloscope would capture a few points on a data bit each time it triggered on the clock and gradually build up a picture of the data (Figure 1A). A recent improvement in technology allows a serial data analyzer to trigger just one time and capture up to 8,000,000 (2^{23}) continuous bits in a data stream, recover the clock timing and place all eight million bit shapes into the eye pattern (Figure 1B). This has several advantages. The first is speed of execution. The purpose of an eye pattern test is to find rare events that violate the test mask, sometimes the test required hours in order to acquire enough data. A second advantage is improved accuracy. In the former method of measuring eye patterns, the trigger jitter of the oscilloscope affected each acquisition. In the newer method, the position of each data bit is referenced to the recovered clock—not to the scope trigger—so the effect of trigger jitter is eliminated. A third advantage of the new method of performing an eye diagram test is that it allows the engineer to locate each and every data bit that failed the test. The acquisition instrument digitizes the full data pattern using an ADC and 100 million points of acquisition memory. Thus the entire eight million bits can be captured seamlessly, with zero dead time in a highly accurate fashion using up to twelve ADC samples on each bit. Bits which violate the test mask can be located and their position in the bit stream gives the engineer the insight to discover why the transmission failed. A final advantage of this acquisition method is that it does not require a clock. In many test situations the clock is not available and in the past the test instrument would use a hardware circuit to recover the clock. This additional electronics added some additional noise/jitter to the timing between the clock signal and the data bits. In the new acquisition method, the same sort of clock recovery filters and gates are applied to the signal mathematically rather than through hardware. As a result, the clock is recovered without adding jitter. An examination of Figures 1A and 1B shows that the older method adds considerable jitter—the jitter added by the test instrument obscures the actual jitter in the signal. Using the new method the real jitter in the signal is seen and the test instrument reveals a much more accurate eye diagram.

Jitter Testing

As bit rates become higher the timing budget gets tighter. The unit interval for a 2.5 Gbit signal is only 400 psec. The purpose of the jitter test is to make sure that no bit is arriving too early or too late compared to its specified time. Though some amount of jitter is allowed, newer standards may allow jitter of only 50-75 psec. Typical tests are for the stability of the period, half period and cycle-to-cycle timing, but a variety of other timing parameters can also be testing. Jitter is a statistical phenomena so the best jitter tests acquire lots of data, and ensure they have captured all the relevant bit patterns in order to assure that jitter due to intersymbol interference, duty cycle distortion and other pattern dependent characteristics have been adequately tested. One method is to simply acquire a very large number of short data records, in the hope that among the many records, each type of data pattern will be captured. A better method is to use the long memory of a serial data analyzer to capture every bit in a test pattern of up to eight million consecutive bits and then apply the jitter test to this data set. The instrument can then compute the jitter, separate it into random (caused by noise) and deterministic (caused by characteristics of the design) components. The deterministic jitter can be further quantified as ISI (intersymbol interference), DCD (duty cycle distortion), PJ (periodic jitter) and BC (bounded component). The engineer can verify if a transmitter has passed the test, or if it fails, he will have information concerning the exact type of failure. This is a particularly useful technique for serial ATA, PCI Express and other serial data formats that use a spread spectrum clock. It is quite likely that worst case timing many occur when the spectral spreading causes particular short or particularly long bits. The user can be certain of capturing these bits by capturing a long continuous data set.

In making a jitter measurement it is important to base the quantitative analysis on a data set that is large enough to be statistically significant. The cohort of measurements should be large enough to have a reasonable confidence of capturing worst case jitter and also large enough to capture the signal of all conditions of operation. For example in testing the variation of bit width data captured over several cycles of the spread spectrum clock is more likely to find the full range of jitter than if only a few hundred bits are captured. Figure 2 shows the difference between the histogram of jitter for capture of 300,000 bits compared to 250 bits. In the case of the shorter capture length, the frequency of the clock can be assumed to have a single value while in the longer duration capture a software PLL is used to track the slowly changing frequency of the clock—in the same fashion as the PLL in an actual receiver would track the clock. The longer set of data does a much more accurate job of measuring the jitter in the same way that a receiver will see it.

Parametric Tests

To perform a complete conformance test to be certain a signal is meeting the specific requirements of a transmission standard, each data transmission protocol specifies the testing of key parameters in the signal. Oscilloscopes and serial data analyzers can measure a wide variety (more than 100) signal parameters. The newest systems even allow the user to create parameters (company proprietary measurements or measurements applicable to new protocol for example) and insert them into the measurement system. Such custom measurements can be created in MATLAB, Mathcad, by writing a Visual Basic Script or even by typing an equation in Excel. This method is much more efficient than moving all the data out of the digitizing application and into the third party math package. Also, it enables the engineer to apply all of the tools of the oscilloscope to the custom calculation. A custom parameter can be histogrammed, an oscilloscope trace can be created that tracks the value of the parameter (allowing the user to zoom in on the part of the acquisition waveform where unusual values of the parameter occurred), etc. Typical parametric tests of optical signals include extinction ratio (how bright is the light of a “1” compared to a “0”) and Q factor (a measure of the timing spread of bit widths). Typical parameter tests of electrical signals are overshoot, undershoot, and amplitude. Figure 3 shows a conformance test for a PCI Express signal. The serial data analyzer captures a long set of continuous bits, capturing every bit in the test pattern over multiple cycles of the spread spectrum clock, and then performs a mask test, computes a jitter bathtub curve, displays the distribution of the bit edges, also displays the distribution of TIE (time interval error—which compares the position of each data edge to its proper position) and also computes four customized parameters. The customized parameters are the eye width, peak amplitude, average bit width and peak bit width jitter.

Summary

New faster standards of data transmission require more accurate test instruments. This need is met by new technology for analyzing serial data streams by capturing a long continuous set of bits makes it possible to raise the confidence level that all bits in the test pattern were captured and that the full cycle of a spread spectrum clock has been examined. This technique raises the confidence level that the device under test really meets (or fails) the requirements. By using an exceptionally strong processing engine, the LeCroy X-Stream technology, the instruments can quickly compute all the standard or customized parameters required, can compare all the data bits to the test mask and it can perform these tests more accurately than previously possible. No trigger jitter is added and the use of a mathematical clock recovery rather than the older hardware method adds no jitter to the clock/data timing.

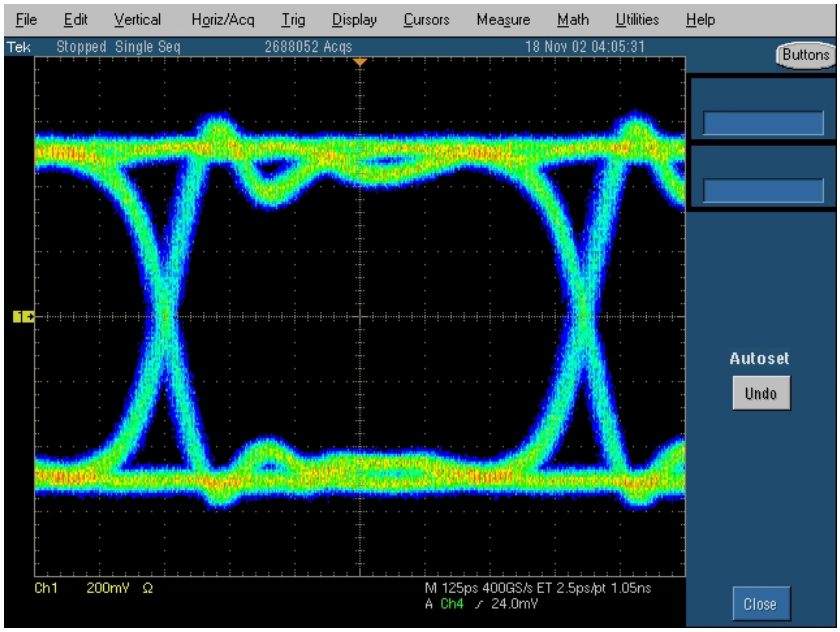

Figure 1A: An eye diagram acquired using many triggers, each acquiring a single bit into the persistence display. A hardware circuit is used for clock recovery. The trigger jitter and hardware clock recovery noise are added to the actual signal jitter.

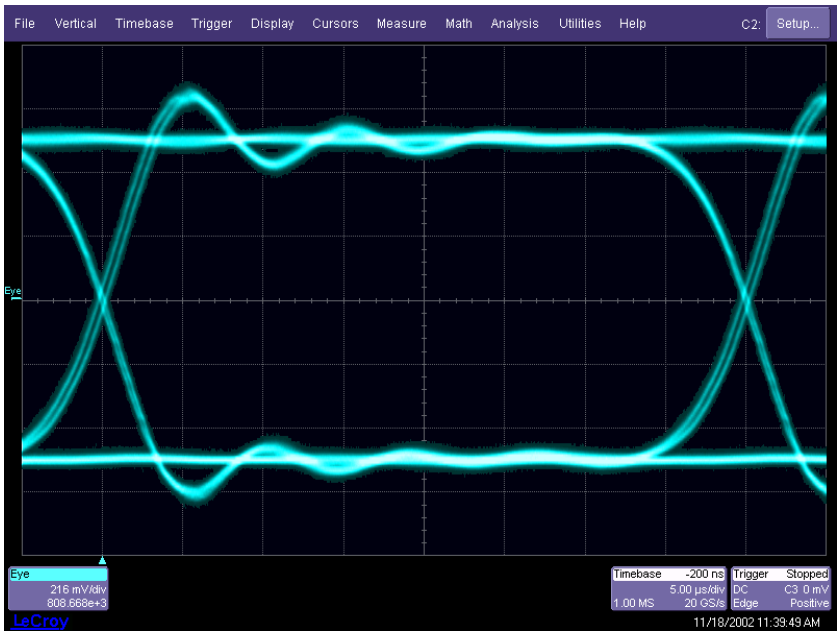

Figure 1B: The same signal acquired using a single trigger to acquire a continuous data set of many bits. There is no trigger jitter, mathematical clock recovery is used and the true eye diagram is much cleaner than figure 1A. Note that a clear view of edge displacement due to intersymbol interference is see in the separation of the rising edge.

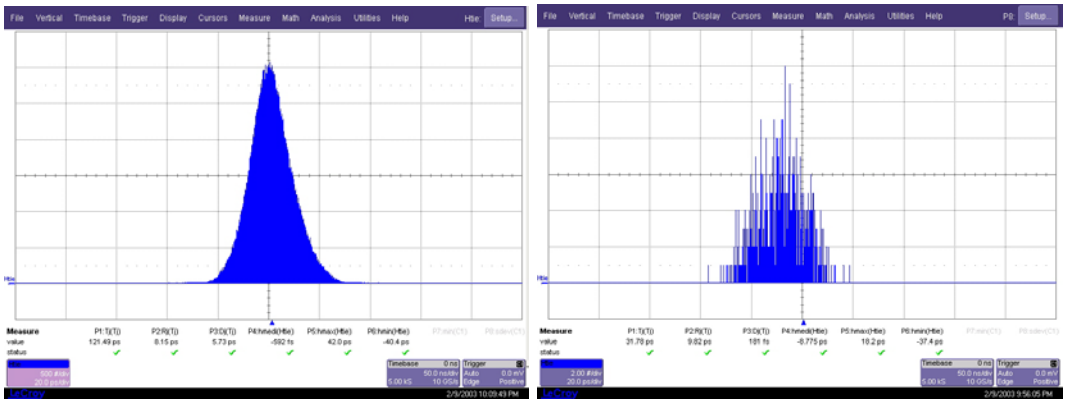

Figure 2A/B: Jitter histogram of 300K bits using software PLL (left) and 250 bits using fixed frequency estimate

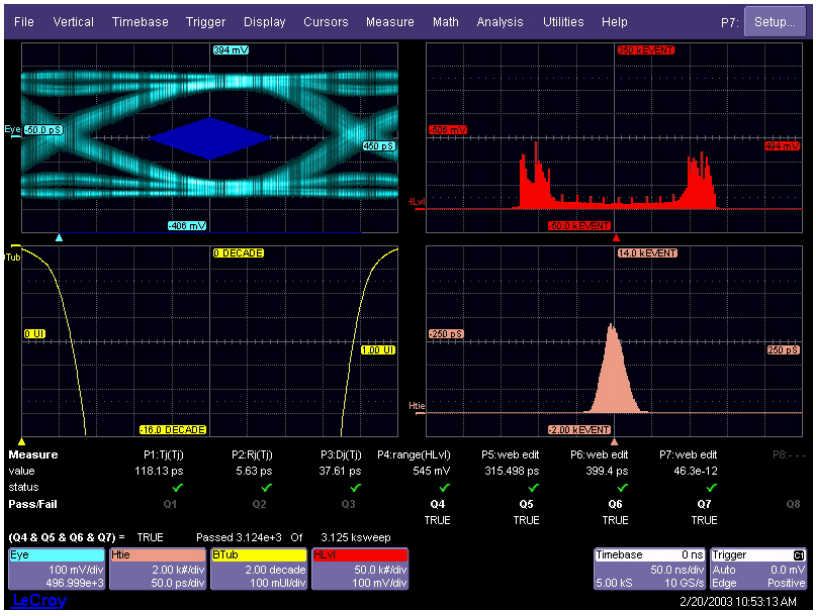

Figure 3: A PCI-Express conformance test. Note the 4 tests in the lower right hand corner show maximum amplitude (545 mv), eye opening (315.5 psec), average bit width (399.4 psec) and worst case jitter (46.4 psec). The screen also shows as mask test, jitter bathtub curve, T, (total jitter) Rj (Random jitter) and Dj (Deterministic Jitter).